DESCRIPTION

SEMICONDUCTOR PACKAGE AND STACKED SEMICONDUCTOR PACKAGE

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TECHNICAL FIELD

The present invention relates to thin semiconductor packages and three-dimensionally stacked semiconductor packages, and more particularly, to a semiconductor package and a stacked semiconductor package with an improved package structure which can facilitate packaging of semiconductor devices regardless of the number of input/output leads thereof.

BACKGROUND ART

Figs. 22 through 25 are sectional views showing the conventional semiconductor packages described in Japanese Patent Laid-Open Publication No. Hei 8-335663. The semiconductor device shown in Fig. 22 is constructed such that electrode pads 504 of an interposer substrate 502 which has a patterned wiring 505 and an insulating film 510 laminated on both surfaces of the patterned wiring 505 are connected to the electrodes of a semiconductor chip 501 via conductors 503. Then, an insulating resin 509 is inserted in between the interposer substrate 502 and the semiconductor chip 501. Subsequently, the interposer substrate 502 is folded from the side surfaces to the rear surface of the semiconductor chip 501, and the insulating resin 509 is applied to an area of the rear surface of the semiconductor chip 501 at which the chip surface is exposed, thereby adhering the interposer substrate 502 to the